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Steven Fischman, ESQ.
Scully, Scott, Murphy and Presser
400 Garden City Plaza
Garden City, NY 11530

EXAMINER	
PADGETT, MARIANNE L	

ART UNIT	PAPER NUMBER
1792	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,647	CHOE ET AL.	
	Examiner	Art Unit	
	MARIANNE L. PADGETT	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11, 13-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. **Claims 1-11 & 13- 24** are rejected under 35 U.S.C. **112, first** paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicants have added the limitations to all three of their independent claims, citing [0019] & [0043] on page 9 of their response as support therefore. The examiner notes that the addition of "an oxidizing environment" defining the "annealing...to form a silicon-on-insulator structure..." is clearly supported from original claims 18-20 & paragraphs [0043-47] in the body of specification, the application of a annealing step in a hydrogen containing ambient after formation of the SOI structure, lacks support in the breath claimed. It is noted that **[0019],** [0034] & [0052-54] discuss a hydrogen bake step in a hydrogen ambient that corresponds to claims 10 & 11 and takes place after providing structure with vacancies or voids, but before ion implanting (is for desorbing impurities & closing surface pores). However, **[0020]** referring to the embodiment described in **[0048]** is the closest support for the new hydrogen annealing limitation added to all the independent claims, requiring "annealing the silicon-on insulator structure in a hydrogen containing ambient", but this post oxidation process step is only relevant when excess dopant ions have been implanted, then it is used for the purpose of reducing levels of dopants within the silicon-containing overlay. Since none of the independent claims **have any dopants ions** required to be present/implanted, thus none which might be in **excess needing removal**, there is neither any point, nor any support for broadly performing the post oxidation thermal anneal in a hydrogen ambient, as taught in [0048] for the claims as presently written. For this reason these claims encompass **New Matter**.

Claims 1, 4-11 & 13-24 now are rejected under **35 U.S.C. 112, first** paragraph, because the specification, while being **enabling for** performing the post oxidation hydrogen anneal when dopant ions that might be in excess are present, does **not reasonably provide enablement for** performing the

post oxidation hydrogen anneal without regard to whether or not any dopant ions that need excess removed are present. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. Particularly see preceding discussion

Given the purpose of the post oxidation hydrogen anneal, the examiner considers the new hydrogen annealing limitation to have enablement when combined with claims 2-3, which require the presence of n- or p-type dopants (and also would be in claims 4-6 if as disclosed in the specification [0028] the electrolytic anodization was claimed to be employing doped structures), however the support is minimal/questionable in that these dependent claims don't require actual ion implantation of the dopant nor that excess dopant be present, although as disclosed in [0027] the doping may be by ion implantation.

2. It remains relevant that the requirement in all independent claims concerning the region of vacancies or voids being porous **must** consider this with respect to what applicants mean by **"porous"**, which is **further** limited by claim 7, where this **dependent** claim states "said porous region of vacancies or voids has a **porosity of about 0.01 % or greater**". Note this claim is consistent with the original specification [0013], which states "a large concentration (**on the order of about 0.01 % or greater**) of vacancies or voids. The terms **'vacancies' and 'voids' are interchangeably** used in the present invention to did now at a porous Si region" (emphasis added), hence porous must be read in light of both the specification & dependent claim 7. Note as "on the order of about" might be considered to be make the defined range of the specification slightly broader than that of dependent claim 7, dependent claim 7 will not be considered to be not further limiting to the independent claim. For these reasons it was previously noted that rejections over Sadana et al. (5,930,643) or Norcott et al. (6,486,037 B2), were not removed as the processes therein were directed to creating vacancies, as an interstitial vacancies, although the disclosures did not discuss creating porosity.

While the examiner finds it doubtful that porosities as low as about 0.01 % (0.01 void volume/100 parts total volume) would be called porous by most people or one of ordinary skill of the art, that **as claimed** the porosity region of the independent claims may have a porosity of 0.01 % (i.e. a density of 99.99 % of theoretical) or even lower porosity, since the dependent claim is required to further limit the independent claim, thus the independent claims porosity region necessarily includes **porosity** of <0.01 % (i.e. 0.009, or 0.001, etc.), as all greater porosities are encompassed by the necessarily narrower range of the dependent claim. Considering the claimed & defined values, plus the taught interchangeability of vacancies & voids in the specification for the present invention, the examiner must conclude that it is the intent of the application as filed to include substrates having vacancies, such as interstitial vacancies or defects, as being considered porous, thus upon reconsideration in light of the specification, the examiner cannot consider the amendment of the independent claims to include the description of "porous" inserted before "region of vacancies or voids" to make any difference in the scope of the claims.

The references of Ulyashin et al. (6,806,171 B1: col. 4, line 62-col. 5, line 67, especially lines 1-5 & 54-60 calling 1-10% low porosity); Balucani (2008/0012114 A1: [0103-104] defining needs for calculating porosity & considering relatively low porosity to be lower than 40 %) and Siuzdak et al. (6,288,390 B1: col. 11, line 4-col. 12, line 48 teaching a minimum porosity of 4 % for silicon to be porous) remain instructive for teaching what is commonly considered porous or low porosity, however as applicant has been their own lexicographer, for purposes of examination we must consider the values as defined by applicants' specification.

3. **Claims 18-22** are rejected under 35 U.S.C. **112, second** paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claim 1, from which claims 18 & 21-22 depends, has been amended to add another "annealing..." step, however these claims have not been modified to clarify to which annealing step is being referred, such that their meanings may now be considered ambiguous, since the claim language now does not clarify when/which step is being further modified.

Additionally with respect to claim 18 & its dependents 19-20 (assuming the original & first annealing limitation), the "an oxygen-containing ambient" lacks a clear relationship to the "an oxidizing environment", which was added to the independent claim. Would insertion in claim 18 after "preformed in" of -- the oxidizing environment, which is --, provide applicants intended meaning?

4. The following is a quotation of the appropriate paragraphs of **35 U.S.C. 102** that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of **35 U.S.C. 103(a)** which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of

each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims **1-11 & 13-25** are rejected under 35 U.S.C. **102(e)** as being anticipated by **Bendernagel et al. ((6,800,518 B2)**, which incorporates PN **5,930,643 to Sadana** et al. by reference), as discussed in section 7 of the action mailed 6/14/2007.

The applied reference has a common assignee & overlapping, but not identical inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Applicants have not met the above stated criteria, nor have they presented any other sufficient arguments to overcome this rejection with respect to by **Bendernagel et al**. (6,800,518 B2), since they are supplied 131 affidavit was defective. See discussion in section 2 of the action mailed 4/8/2008.

Applicants have added a requirement for a **hydrogen ambient anneal** after formation of the silicon-on-insulator structure, however Bendernagel et al. (518) particularly teach such a step on col. 9, lines 40-50 sequential to the high-temperature oxidation anneal, teaching that "During the high-temperature annealing step, dopants present in substrate 10 may defuse from substrate 10 into the Si over-layer 30. If the level of doping concentration in Si over-layer 30 is too high, for a given device application, the structure shown in FIG. 1 may be subject to a post hydrogen annealing process. The post hydrogen anneal includes the same or different conditions as that of the optional hydrogen anneal mentioned above. A preferred post hydrogen anneal that may be employed in the present invention is a

0.25-3 hour anneal in low-pressure (82 Torr or less) hydrogen ambient at 1100-1150°C." Therefore the new limitation added to the claims by applicants is clearly covered by the disclosure of Bendernagel et al.

As previously discussed, Bendernagel et al. teach forming composite structures, which may include buried insulators (oxides), buried conductive & buried void plane structures, by forming a layer of porous silicon (or alternately forming vacancies or voids) in the surface region of a semiconductor substrate, such as silicon via electrolytic anodization with a HF-containing solution, where the porosity produced is mainly dependent on the current (~0.1-20 mA/cm^2) & voltage (~0.1-10 volts typical, ~0.5-5 volts preferred) used, the HF concentration, and the dopant type & concentration in the wafer, and where thickness of the porous silicon layer may additionally depend on the time (~30 sec.-10 min.,~1-5 min. more highly preferred) of anodization process. For this process Bendernagel et al. teach that the "semiconductor **wafer needs to be doped**, preferably but not necessarily with **p-type** doping atoms. When a **boron**-doped p-type wafer is employed, the dopant concentration of the wafer is typically from about 1E15 to about 1E19 atom/cm^3..." (emphasis added, col. 6, lines 18-26). Next it is taught that a brief anneal in hydrogen ambient at elevated temperatures may be employed to eliminate open pores on the surface of the porous silicon layer, thereafter an epitaxial silicon (epi-Si) layer on the surface, then the composite substrate is ion implanted, where the ions employed may be oxygen ions, when a buried oxide is intended, or optionally may include nitrogen ions, or just nitrogen ions for an alternate buried insulator, or metal ions for a buried conductor or void planes. Masking may optionally be employed, with a HF-resistant material (photoresist) before the anodization step &/or a patterned mask for selective ion implantation before implanting, which masks are removed before deposition of the epi-Si or after ion implanting, respectively. Oxygen ion implanting may be in a single or multiple steps, continuous or pulsed, or combined with other ion implantation steps depending on desired structure. Oxygen implanting is taught to be via any conventional ion implantation apparatus, with any conventional ion implanting conditions employed, which are exemplified as O-ion dose from about 1E16-2E18 atoms/cm^2,

implantation energy from about 50 KeV-10 MeV, ion beam current density from about 0.05-500mA/cm^2, and ion implantation temperature from about 480-650°C. More preferred oxygen ion implantation conditions are also given (~5E16-2E17 atoms/cm^2, ~150-300 KeV, ~1.0-10 mA/cm2, ~550-600°C) as well as this high-temperature ion implantation step followed by a normal room temperature ion implantation step exemplified in prior art references. After the ion implanting step(s) high-temperature annealing is performed to transform the implanted oxygen regions into buried oxide regions, while regions that do not contain oxygen ions can be transformed into buried void layers or buried conductive regions. The high-temperature annealing in is performed at temperatures of about 1300°C or greater, but less than the melting point of Si , which is 1415°C, and may be carried out it atmospheres of pure oxygen (O_2), oxygen mixed with an inert gas or N_2, or either without oxygen, or vacuum. When annealing causes significant diffusion of dopants into the overlying silicon layer, a post hydrogen annealing process, which may use the same or different conditions (0.25-3 hours, ≤ 82 Torr H-ambient, T = 1100-1150°C) is then employed. Col. 9, lines 7-12 note that during annealing the porous silicon is consumed by the formation of the buried oxide/void, and that the epi-Si layer may be thinned by surface oxidation.

Bendernagel et al. teach that the thickness of various layers of the composite structure may vary depending on process conditions employed during fabrication, where typically the buried insulating region has a more highly preferred thickness from about 5-200 nm, and that the thickness of the buried insulating regions is dependent on device requirement and could be controlled by adjusting vertical depth of the porous silicon layer form during HF-anodization and the dose of the implanted ions. Particularly see the abstract; col. 2, lines 58-68; col. 3, lines 20-30 & 40-col. 4, line 44; col. 5, lines 10-15 & 27-39; col. 6, lines 17-col. 10, line 40, especially col. 6, lines 17-col. 7, lines 8 for doping & anodization, col. 7, lines 9-31 for H-anneal to eliminate open surface pores, col. 7, lines 32-44 for the epi-Si layer, typically monocrystalline structure ≡ single crystal, col. 7, lines 45-67 for masking, col. 8 for ion implanting & col. 9 for annealing.

With respect to applicants' claim 17, which is directed to specific parameters for a second oxygen implantation step, it is noted that Bendernagel et al's teachings on col. 8, lines 15-31 can be said to overlap with these parameters for their taught second implantation step at a normal room temperature, which is in the claimed temperature range for the second oxygen implantation, assuming that the other parameters employed for the second implantation can be any of the preceding taught parameters, which are overlapping with those claimed, or as suggested one may look at the exemplary art, such as USPN 5,930,643 by Sadana et al., which was **incorporated-by-reference**, that teaches forming buried oxide layers by creating a damaged buried region in a semiconductor substrate (Si) via oxygen ion implantation, possibly through a capping layer, using a low-dose ion implantation (~≥5E16) at high temperatures about ≥ 200°C, plus a second yet lower ion dose implantation at same or different energies carried out at cryogenic temperatures to about 300°C at doses of about 2E14-4E15 ion/cm^2. The ion implantation in Sadana et al. is followed by an oxidation step typically carried out in an inert ambient (N_2 or Ar) mixed with oxygen at temperatures from about 1300°C or higher, with optional further annealing of the oxidized structure (col. 2, lines 10-43), thus providing specific parameters for the two-step oxygen ion implantation alternative, which read on claim parameters and which are employed with oxidation & annealing procedures as taught and claimed.

6. Given its relevance due to incorporation discussion concerning Sadana et al. (643) is repeated below. Also discussion in section 2 above concerning porous & porosity as read in light of the specification, remains relevant, especially considering claim 7, such that the substrates' that have been treated to create vacancies must be considered inherently porous in light of applicants specification.

Applicants have previously argued (page 8 of 10/15/07 response) that oxygen ion implantation does not expressly or inherently caused voids in semiconductor substrates, but may provide amorphization, however given the definition of porous and applicants specification, as voids are claimed in the alternative with "vacancies" & taught in the specification to be equivalent, which one of ordinary

skill in the art would clearly consider to be encompassed by the taught defects or damaged regions of Sadana et al. (643), as was previously discussed & not contradicted by the claim language as defined, and as vacancies are a type of defect or damage inherently caused by ion implantation, thus considered to be equivalent concepts or semantics differences.

As noted above & previously, Sadana et al. (643) has all the parameters to the claimed oxygen ion implanting & annealing steps, for producing buried oxide layers of thicknesses claimed. While Sadana et al. does not discuss providing a silicon-containing semiconductor material in the substrate that has a region with "vacancies or voids located therein" the initial ion implanting step which creates **defects with inherently include defects that may be described as "vacancies",** as created defects would have been expected to include displacements of atoms in the silicon-containing substrate, thus vacancies. Further note that while Sadana et al. (643) most explicitly discuss a 2-step procedure, their teachings are inclusive of "this low temperature/low dose ion implantation step may be carried out in either a single step with a single temperature or multiple steps with multiple temperatures, which range from about cryogenic to about 300°C or less", such that the multistep ion implantation procedure described thereby reads on applicant's claimed process, even if one considers the "providing..." step necessarily separate from the step of "implanting...", as the multistep sequence to produce the low temperature low dose implantation, encompasses or overlaps with those sets of applicants' oxygen ion implantation parameters.

As previously discussed, claimed temperatures for two oxygen ion implantations relate to Sadana et al. (discussed above), who is also directed to creating buried oxide regions in semiconductors via oxygen ion implantation, where the desirability of providing two different effects (buried **damage region** & **adjacent amorphous** layer) via use of two ion implantations differentiated by dosage & temperature, is taught for controlling resultant oxide thickness & properties (col. 2, lines 1-43+; col. 4, lines 7-29 for first ion implantation & lines 30-65 for second ion implantation; col. 6, lines 8-16 note that the **defect containing amorphous region** is believed to enhance oxygen diffusion into the silicon & combine with

the first created damage layer during the annealing step to form the buried oxide region; figure 2 & col. 6, lines 47-59 this 2-step 2 temperature ion implantation taught to improve electrical & structural qualities of oxide layer & save implant time & wafer cost), hence noting claimed parameters & claimed multiple ion implantations as discussed in Sadana et al. for taught advantages in producing analogous buried oxide layers using analogous ion implantation with analogous subsequent annealing techniques. Also note that exemplary buried oxide region thicknesses via Sadana et al.'s process include 1000 Angstroms, i.e. 100 nm (example 1, specifically col. 7, lines 60-62), relate to claimed thicknesses for buried oxide layers in semiconductor substrate constructions.

7. **Other art** of interest includes Sato et al. (5,854,123) who is also performing ion implantation processes in conjunction with making SOI structures, and discusses annealing under hydrogen atmosphere, however this is after ion implanting with hydrogen ions (e.g. Ex. 6, col. 28, etc)., thus the hydrogen anneal is not performed in a sufficiently relevant context.

8. **Applicant's arguments** with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed **6/17/2008** & discussed at the have been fully considered but they are not persuasive. It is noted that the rejections in sections 4, 6 & 8 based on **Houston et al**. (2002/0086463 A1), **optionally** in view of Sadana et al. (5,930,643), or **Sadana et al.** (643) alone, or **over Norcott et al. ((6,486,037 B2**), which is the child of Sadana et al. (643), were removed by the addition of the post oxidation hydrogen annealing, since nothing in the procedures taught therein suggested a hydrogen anneal at that point (after formation of the SOI) in the procedure.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. **Any inquiry** concerning this communication or earlier communications from the examiner should be directed to Marianne L. Padgett whose telephone number is (571) 272-1425. The examiner can normally be reached on M-F from about 9:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks, can be reached at (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Marianne L. Padgett/
Primary Examiner, Art Unit 1792

MLP/dictation software

9/28/2008